PATENT

Attorney Docket No.: BEA9-2000-0013-US1

BOARD OF PATENT APPEALS AND INTERFERENCES
IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	McKenney et al.		
Serial No.:	09/753,062	Group Art Unit:	2112
FILING DATE:	December 28, 2000	Examiner:	Huynh, K.
FOR:	**Quad Aware Locking Primitive**		

REPLY BRIEF OF PATENT OWNER ON APPEAL

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicants, by way of Reply, wish to address new issues and comments presented in the Examiner's Answer of June 9, 2006. The Examiner raises issue with the Applicants' argument distinguishing a hierarchy from a priority. Accordingly, Applicants address this point below.

A. Examiner's Grounds of Rejection

While the Examiner accepts Applicants' definitions of hierarchy and priority, with all due respect to the Examiner, Applicants respectfully disagree with the Examiner's position that a priority may be a form of a hierarchy. The Examiner utilizes the *Kermani* reference as the primary reference in rejecting Applicants' claimed invention. However, the Applicants' Response to the Final Official Action and Brief in Support of Appeal distinguished *Kermani.* More specifically, *Kermani* discloses a priority of processors or agents. Applicants' invention

discloses a hierarchy of processors or agents. While the Examiner asserts that a priority may be considered a hierarchy, the Examiner's characterization of a priority, in such a case, lacks the fundamental elements required to form a hierarchy.

Applicants hereby incorporate by reference remarks pertaining to the *Kermani* patent as discussed in the Brief in Support of Appeal submitted March 23, 2006, and directs the Board of Patent Appeals to such remarks as demonstrating the various distinctions between the prior art, specifically *Kermani*, and the claimed invention.

B. *Kermani's* Priority Verses Applicants' Hierarchy

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." [1] With all due respect to the Examiner's position, Applicants respectfully disagree with the Examiner's interpretation that a priority as described in *Kermani* can be a type of a hierarchy as claimed by Applicants. As such, the prior art cited by the Examiner, *Kermani*, fails to describe all of the elements claimed by the Applicants, and fails to anticipate each and every element of the Applicants' invention.

As disclosed in the Brief in Support of Appeal, Applicants' invention includes a computer system with a plurality of processors organized into a hierarchy with instructions to enable a lock to be passed to a waiting processor on an intra-quad basis when appropriate, and passed to a waiting processor on an inter-quad basis when a particular quad has been monopolizing the lock for an extended prior of time. This hierarchical ranking of the processors together with processing the lock responsive to Applicants' hierarchical structure enables equitable access to and distribution of the lock in a heavy contention environment and thereby increases the efficiency of the system.[2] Accordingly, it is this hierarchical relationship between the processors that is central to the Applicants' invention, but it is this hierarchical relationship

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[1] MPEP §2131 (citing *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987)).

[2] See Brief in Support of Appeal, page 2

that *Kermani* lacks.

Kermani discloses that agents or processors are equally placed in a structure with each agent sharing equal access to synchronous memory, *i.e.* the time differential for each lock handoff among processors is equal. Each of the agents may submit a memory access request wherein "a winning agent is preferably selected on a priority level assigned to each of the requesting agents."[3] However, *Kermani* continues by stating: "[p]referably, a unique priority level is established for each of the plurality of agents 100 to 108 either before operation of the system or on-the-fly as the system is operated."[4] In other words, *Kermani* may assign a priority to one or more agents in a system, but the time differential for each lock handoff among the processors remains equal.

In differentiating the Applicant's invention from *Kermani* one must first understand the definitions of both a hierarchy and a priority. A hierarchy was defined as "an organizational technique in which items are layered or grouped to reduce complexity."[5] As Figure 1 of the Brief in Support of Appeal illustrated, a fundamental element of a hierarchy is that multiple items, or processors as in Applicants' invention, are grouped together and organized into positions based upon a hierarchical tree-like structure. Each group in Figure 1 is placed within a tier such that each tier depends upon the preceding tier to access the lock. For example, in Applicants' invention Tier 1 is represented as a level in the hierarchy at the top of the structure with one quad having four processors with one of the processors in possession of the lock. Tier 2 is represented by quads 2a and 2b wherein 2a and 2b have an equal time differential for handoff of the lock from a processor in the quad of Tier 1. The processors in the quads of Tier 3 have a different time differential, *i.e.* greater time differential, for a lock handoff from a processor in the quad of Tier 1 than a processor in one of the quads of Tier 2 as the processors in the quads of Tier 3 are in a different layer in the hierarchy. The processors in the quads of Tier 2 are separated from the quad in Tier 1 by the Tier 2 layer of the hierarchy. The same applies to Tier 4 in that all

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[3] See *Kemani* Col. 4, lines 50-52.

[4] *Id.* Col. 4, lines 52-55.

[5] See Exhibit A attached to Response to Office action Submitted July 21, 2004.

processors in this layer have an even greater time differential for a lock handoff from a processor in the Tier 1 layer as the lock must be passed through their respective Tier 2 and Tier 3 quads and associated processors. Accordingly, the time differential for lock handoff among the processors in one Tier in the hierarchy, *i.e.* intra-Tier, may be uniform, however, the time differential for lock handoff on an inter-Tier basis is not uniform.

The time differential for lock handoff on an inter-Tier basis, *i.e.* inter-quad, exists even if each tier in a hierarchy was limited to a single processor. Each processor would exist within a tier and gain access to the lock only through the intervening tiers. A memory access request from a processor in Tier 4 that requires a lock must be communicated through processor 3a in Tier 3 and then through processor 2a in Tier 2 to receive such access. Therefore, a memory access request from processor 4a has a different latency than a memory access request from processor 3a. This is representative of a hierarchy's ordinary structure known within the art and is representative of the structure of Applicants' invention.

The superiority in rank assigned by a priority does not suggest that the processors ranked have different memory latencies. In other words, each processor in a priority has the same memory latency as all other processors in the priority, but accesses memory in a particular order as determined by each processor's priority. No single processor is dependent on another processor for access to the memory as is the case in a hierarchy. Accordingly, the lack of dependancy that exists in a system utilizing only priority assignment, such as *Kermani*, does not provide for the memory latency inherent in a hierarchical system such as Applicants'.

Although a priority may be incorporated into a hierarchy, this is only true to the extent that a priority sets a rank within a pre-existing layer of processors within the hierarchy. In other words, a priority may be established between the multiple processors of one tier, such as quads 3a, 3b, 3c, and 3d of Tier 3. However, the priority may not exist to the extent that it encompasses the entire hierarchy, as the Examiner suggests, because this would require each processor in each tier to have the same memory latency as all other processors which eliminates the tier structure required by Applicants' hierarchical system. Accordingly, a priority structure encompassing the entire system would eliminate all tiers within the tier structure required for a hierarchical system

to exist.

C. Conclusion

In view of the rejections presented by the Examiner in the Office Action made final, it appears clear on the record that the *Kermani* patent does not anticipate Applicants' invention. Although the prior art patent cited by the Examiner relates to a computer system having shared synchronous memory and a hardware element for controlling access to the shared memory, the priority of the processors and the tools used to control access to the shared memory of *Kermani* are different than the hierarchy claimed by Applicants. Accordingly, Applicants respectfully disagree with the Examiner's characterization of a priority as a form of a hierarchy and submits that the Examiner has failed to show that *Kermani* anticipates every element of Applicants' invention.

Applicants believe that those skilled in the art have failed to solve the problem as claimed by Applicants. Accordingly, for the reasons outlined above, Applicants respectfully requests the Board of Patent Appeals direct allowance of this application and all pending claims.

Respectfully submitted,

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